

SPECIFICATION
FOR
LCM Module

MODULE No:	KD028QVFMA058
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.8 " TFT-LCD contains 240x320 pixels, and can display up to 65K/262K colors.

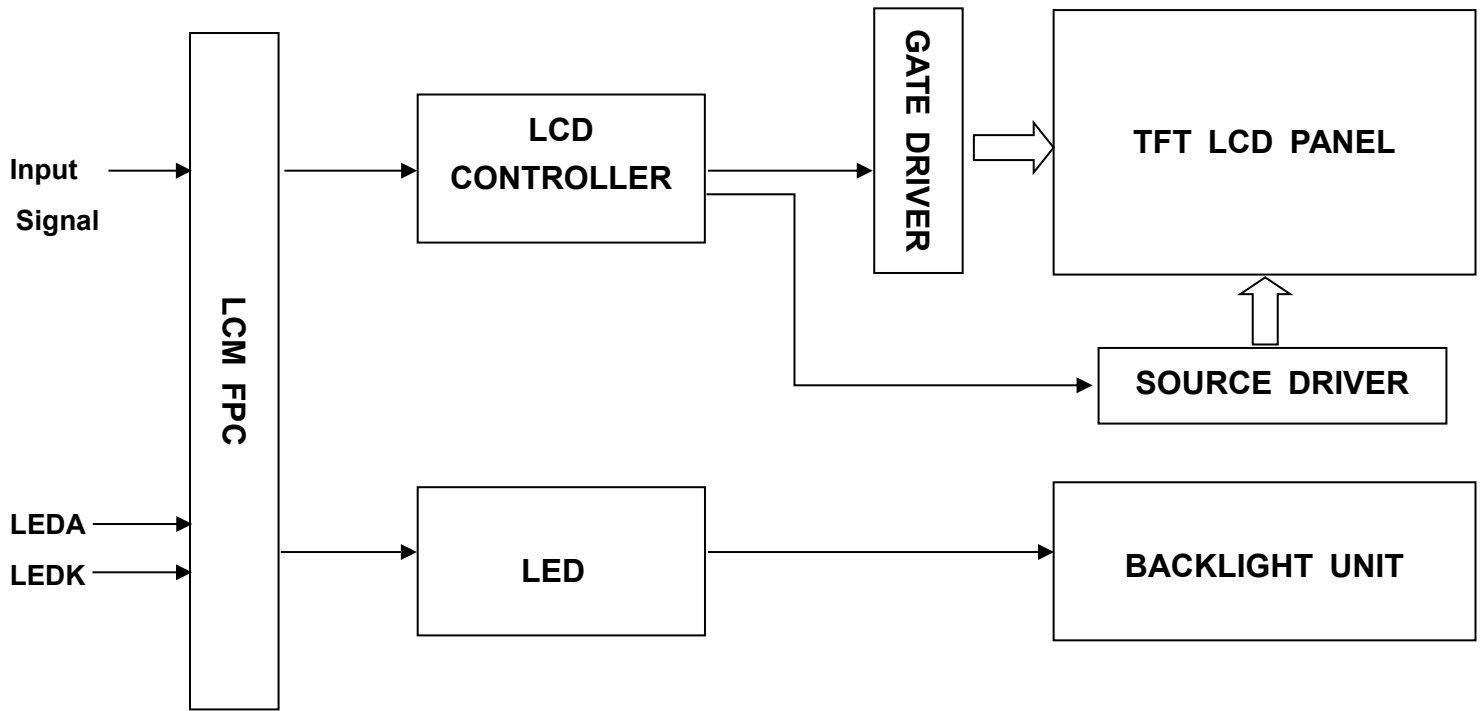
*** Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	43.20(H)*57.60 (V) (2.8inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K	colors	
Number of pixels	240(RGB)*320	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.180(H)*0.180(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	ST7789V2	-	
LCM Interface	8/9/16/18Bit MCU Interface 3/4SPI+16/18Bit RGB Interface 3-line/4-line Serial Interface	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-30~+85	°C	
Storage temperature	-30~+85	°C	

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	50.5	-	mm	
	Vertical(V)	-	69.7	-	mm	
	Depth(D)	-	2.6	-	mm	
Weight		-	18	-	g	

1. Block Diagram



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	XR(NC)	--	--
3	YD(NC)	--	--
4	XL(NC)	--	--
5	YU(NC)	--	--
6	IOVCC	Supply voltage for IO (1.65-3.3V).	P
7	IOVCC	Supply voltage for IO (1.65-3.3V).	P
8	VCI	Supply voltage (3.3V).	P
9	VCI	Supply voltage (3.3V).	P
10	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.	I
11	IM1		
12	IM0		
13	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
14	CS	Chip select input pin ("Low" enable). Fix this pin at IOVCC or GND when not in use.	I
15	RS(SPI-SCL)	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. Fix this pin at IOVCC or GND when not in use.	I
16	WR(SPI-RS)	The data is applied on the rising edge of the SCL signal. Fix this pin at IOVCC or GND when not in use.	I
17	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use	I
18	VSYNC	Frame synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
19	HSYNC	Line synchronizing signal for RGB interface operation.	I

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		Fix this pin at IOVCC or GND when not in use.	
20	ENABLE	Data enable signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
21	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
22	SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.	I
23-40	DB0-DB17	Data bus. If not used pin, fix this pin to GND.	I/O
41	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
42	GND	Ground.	P
43	LEDA	Anode pin of backlight	P
44	LEDK1	Cathode pin OF backlight	P
45	LEDK2	Cathode pin OF backlight	P
46	LEDK3	Cathode pin OF backlight	P
47	LEDK4	Cathode pin OF backlight	P
48	LEDK5	Cathode pin OF backlight	P
49	LEDK6	Cathode pin OF backlight	P
50	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio	CR	$\Theta=0$	800	1000	--		
Response time	Rising	T_{R+T_F}	--	30	35	msec	(1)(2)
	Falling						
Uniformity	S(%)		55	60	--	%	(1)(3)
Color Filter Chromaticity	White	W_X	0.2728	0.3128	0.3528		(1)(4) CA-310
		W_Y	0.3128	0.3528	0.3928		
	Red	R_X	0.5890	0.6290	0.6690		
		R_Y	0.3258	0.3658	0.4058		
	Green	G_X	0.2814	0.3214	0.3614		
		G_Y	0.5637	0.6037	0.6437		
	Blue	B_X	0.1069	0.1469	0.1869		
		B_Y	0.0736	0.1136	0.1536		
Viewing angle	Hor.	Θ_L	75	80	--		(1)(4)
		Θ_R	75	80	--		
	Ver.	Θ_U	75	80	--		
		Θ_D	75	80	--		
Option View Direction	ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25 \pm 2^\circ\text{C}$

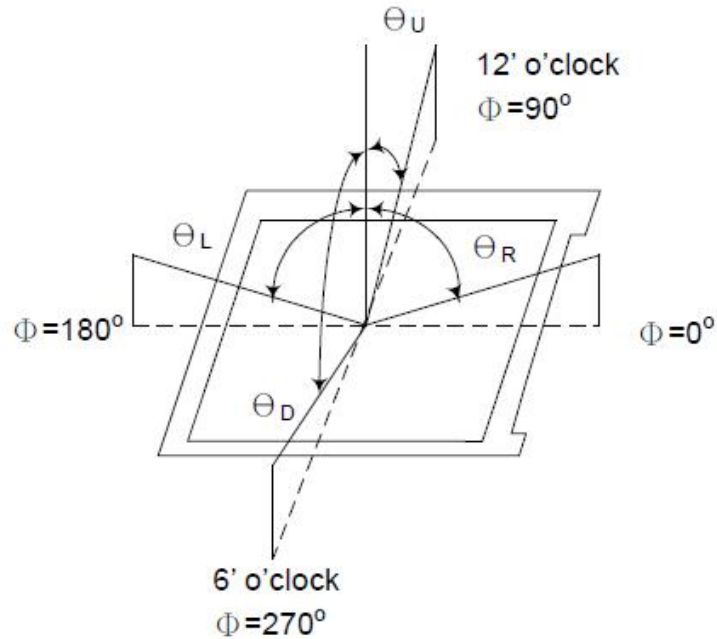
15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

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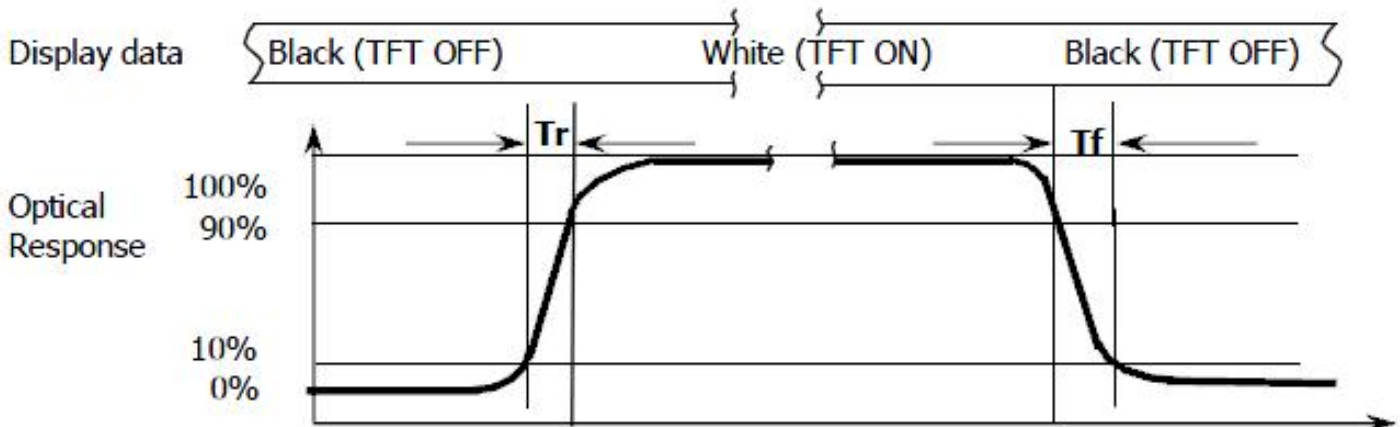
Note (1): Definition of Viewing Angle :



Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

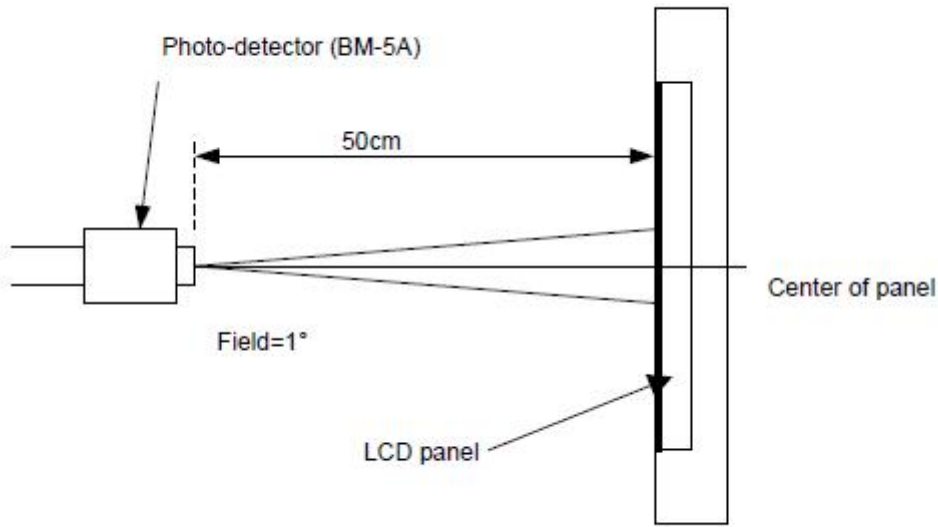
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



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Note (4): Definition of optical measurement setup



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5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	-0.3	4.6	V	Note1
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V	
Operating temperature	T _{OP}	-30	+85	°C	
Storage temperature	T _{ST}	-30	+85	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.4	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current	I _{DD}	--	6	12	mA	
Level input voltage	V _{IH}	0.7*IoVCC	--	IoVCC	V	
	V _{IL}	GND	--	0.3*IoVCC	V	
Level output voltage	V _{OH}	0.8*IoVCC	--	IoVCC	V	
	V _{OL}	GND	--	0.2*IoVCC	V	

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5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips LED

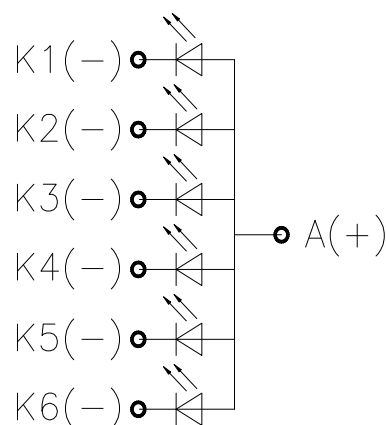
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	90	120	--	mA	
Forward Voltage	V_F	2.8	3.2	3.4	V	
LCM Luminance	LV	650	700	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

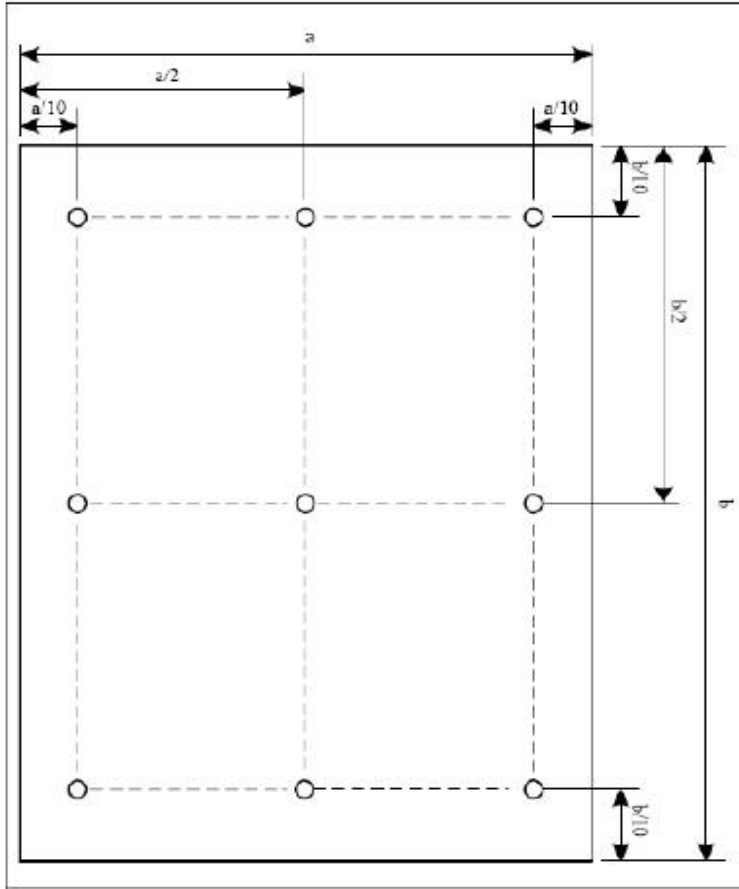
$T_a=25\pm 3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at

$T_a=25\text{ }^{\circ}\text{C}$ and $I_L=120\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 120mA. The constant current driving method is suggested.



Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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6. TFT AC Characteristics

6.1 8080 Series MCU Parallel Interface Timing Characteristics: 18/16/9/8-bit Bus

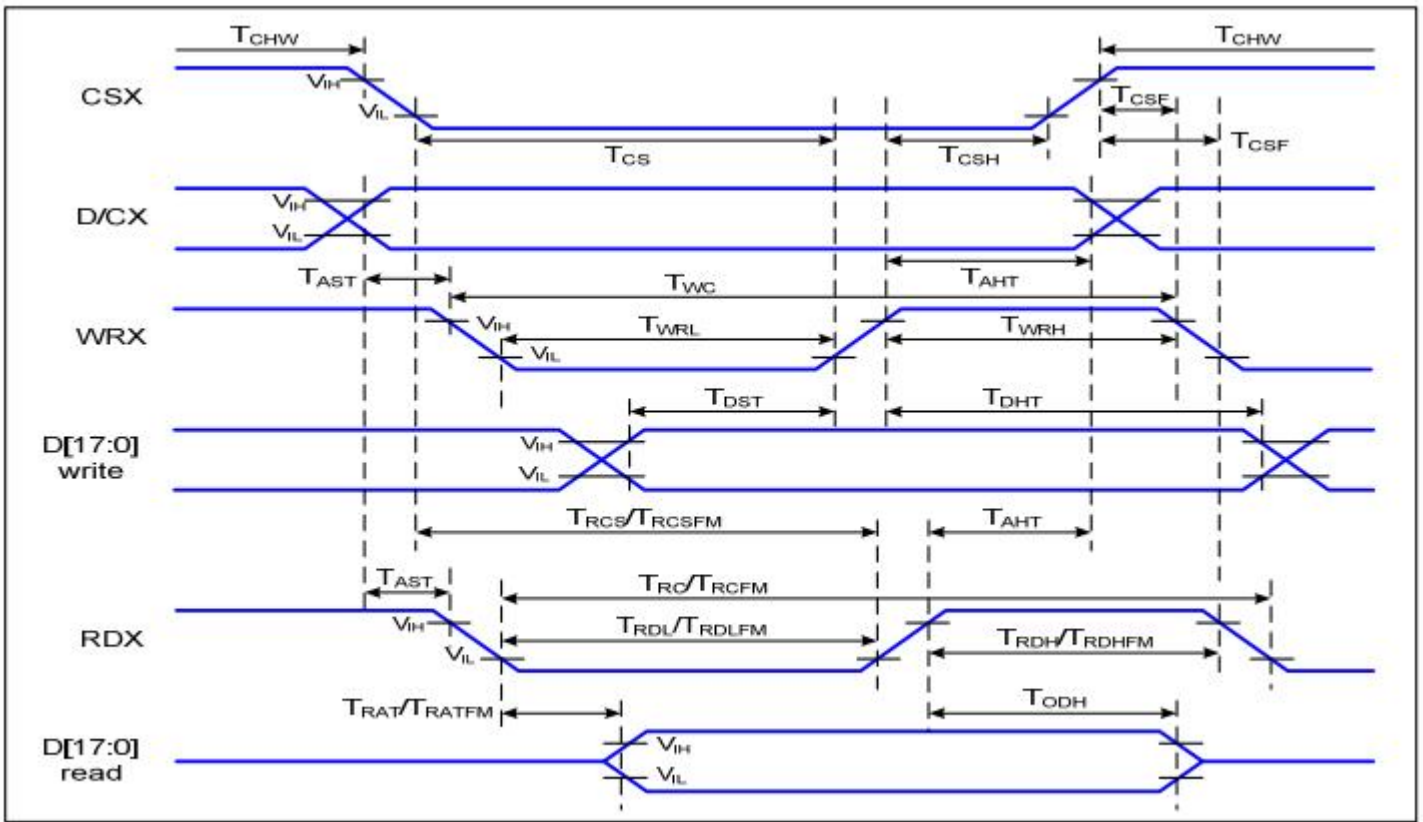


Figure6-1-1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30$ to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse "L" duration	15		ns	
RDX(ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
RDX(FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration(FM)	90		ns	
	T_{RDHFM}	Control pulse "H" duration(FM)	90		ns	
DB[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table6-1-1 8080 Parallel Interface Characteristics

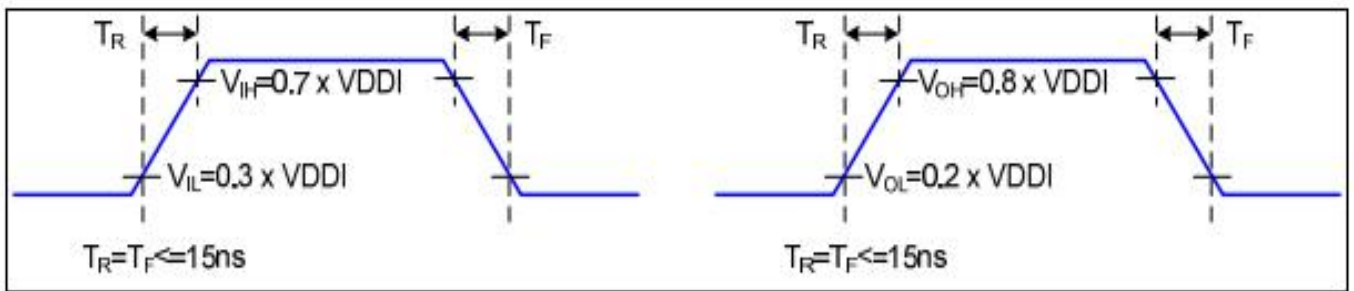


Figure6-1-2 Rising and Falling Timing for I/O Signal

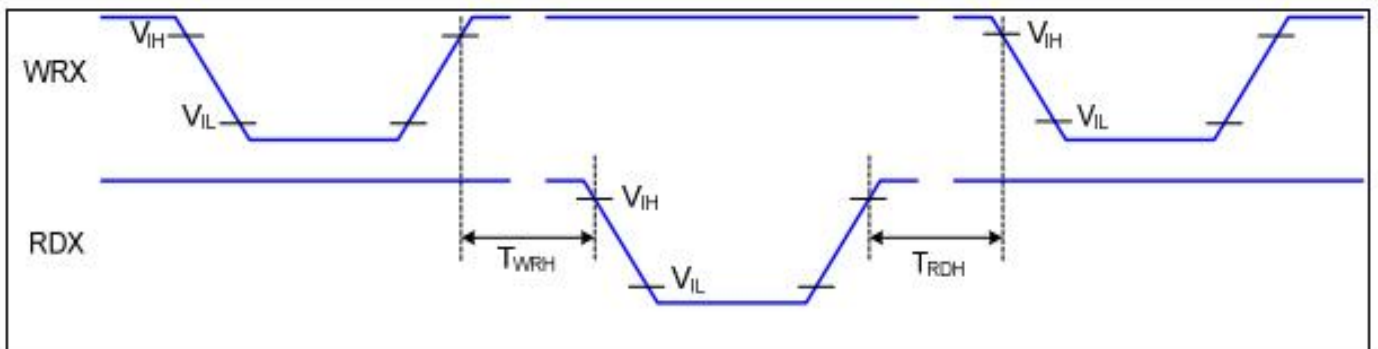


Figure6-1-3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

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6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

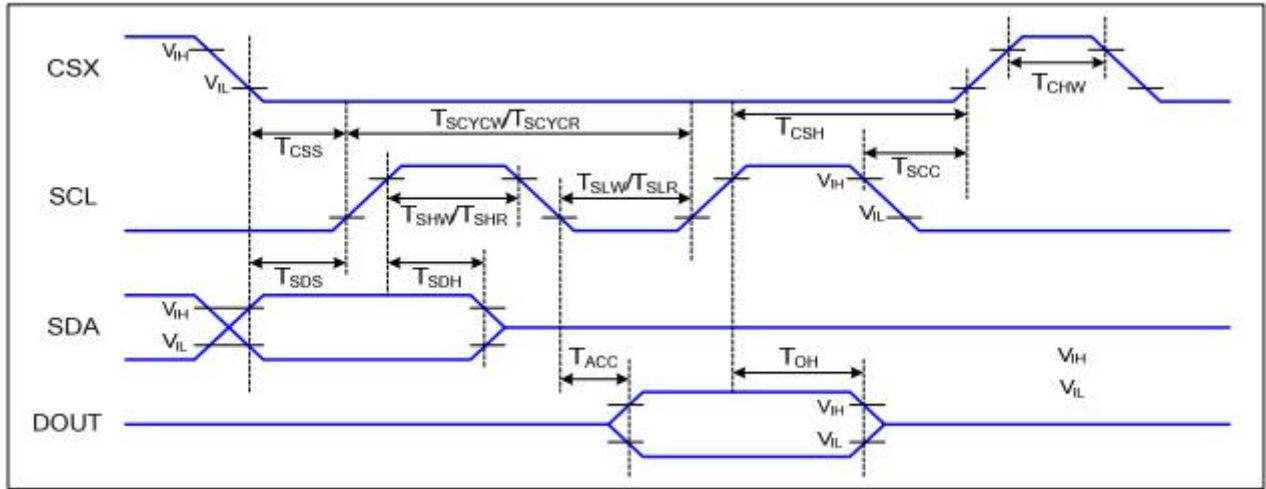


Figure6-2-1 3-line serial Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=-30$ to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (Write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum $CL=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $CL=8pF$

Table6-2-1 3-line serial Interface Characteristics

Note: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

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6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

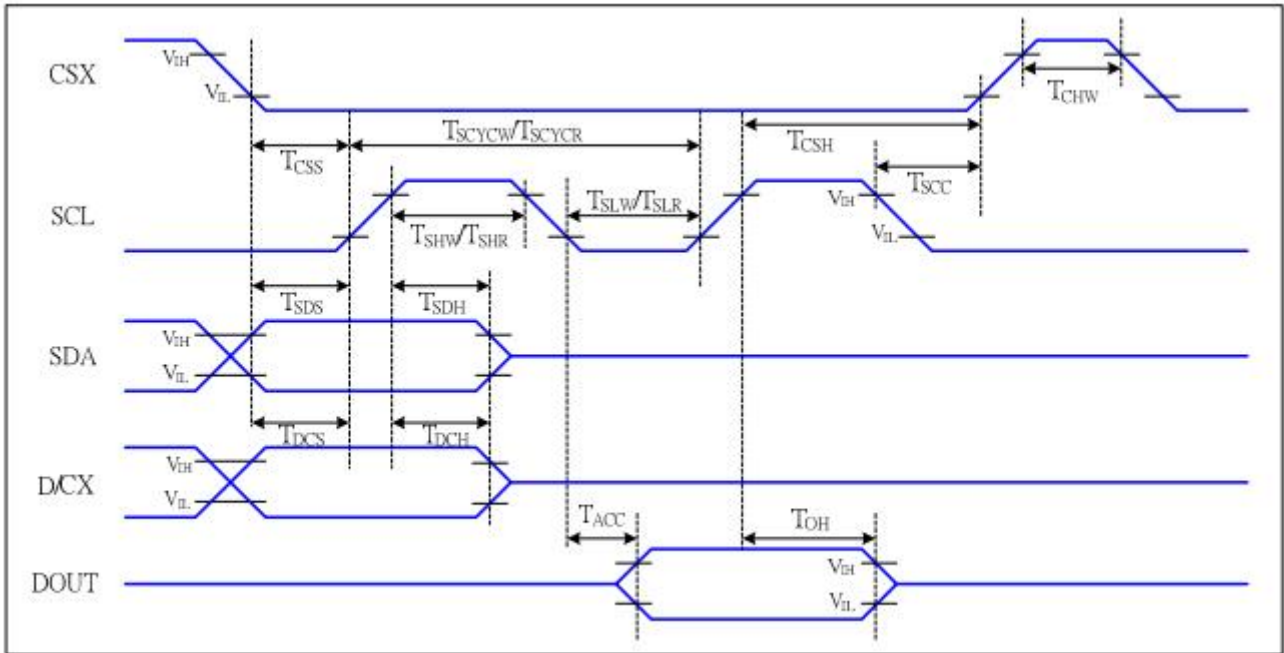


Figure6-3-1 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CSS}	Chip select setup time (Write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T _{SHW}	SCL "H" pulse width (Write)	7		ns	
	T _{SLW}	SCL "L" pulse width (Write)	7		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T _{DCS}	D/CX setup time	10		Ns	
	T _{DCH}	D/CX hold time	10		ns	
SDA	T _{SDS}	Data setup time	7		ns	

(DIN)	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table6-2-1 4-line serial Interface Characteristics

Note: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.4 Parallel RGB Interface Timing Characteristics

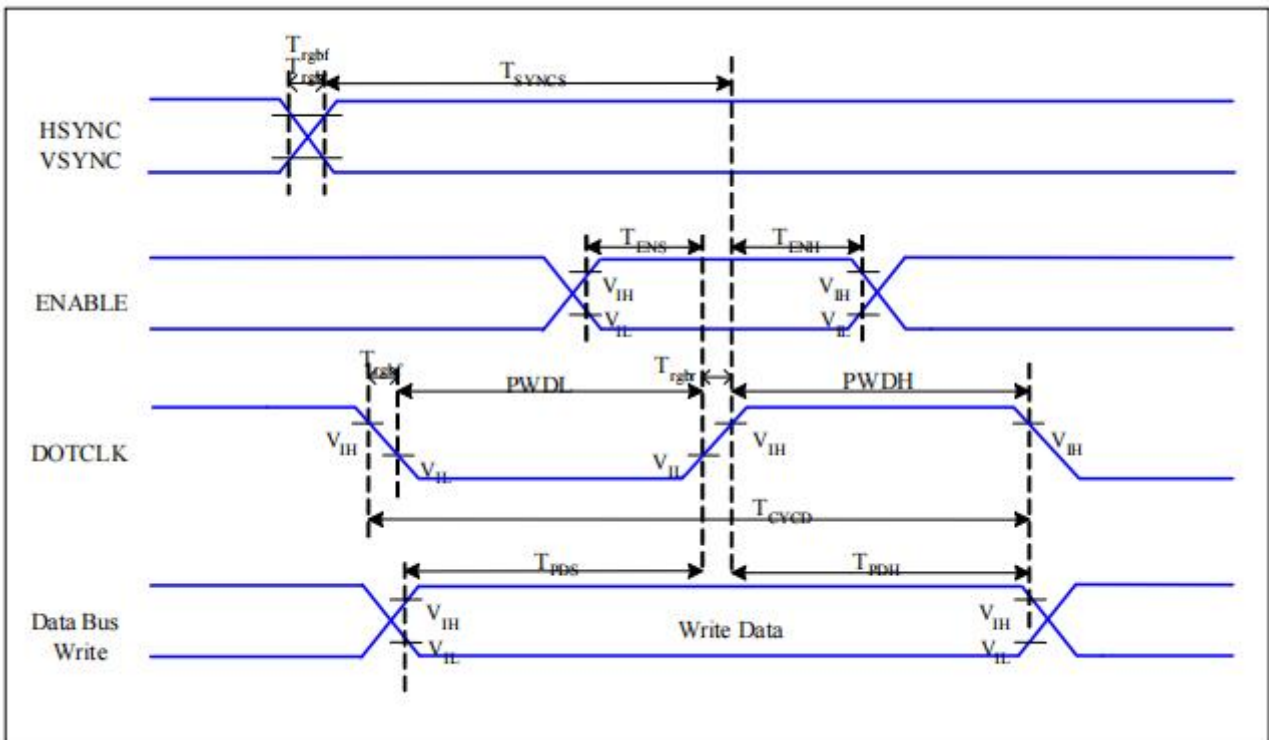


Figure6-4-1 RGB Interface Timing Characteristics

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a = -30$ to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30		ns	
ENABLE	T_{ENS}	Enable Setup Time	25		ns	
	T_{ENH}	Enable Hold Time	25		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60		ns	

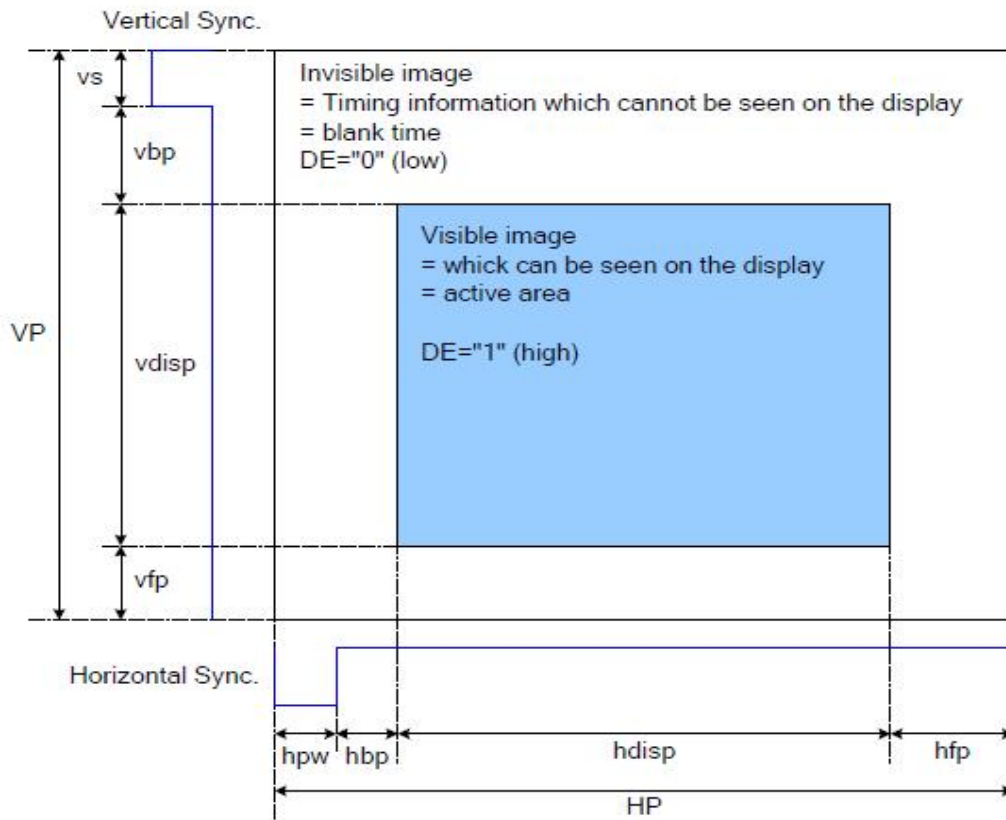
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	PWDL	DOTCLK Low-level Pulse Width	60		ns
	T _{CYCD}	DOTCLK Cycle Time	120		ns
	T _{rghr} T _{rghf}	DOTCLK Rise/Fall time		20	ns
DB	T _{PDS}	PD Data Setup Time	50		ns
	T _{PDH}	PD Data Hold Time	50		ns

Table6-4-1 18/16 Bits RGB Interface Timing Characteristics

6.5 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

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Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	6	--	MHz
Horizontal Sync. Width	hpw	1	2	255	Clock
Horizontal Sync. Back Porch	hbp	1	20	255	Clock
Horizontal Sync. Front Porch	hfp	1	36	--	Clock
Vertical Sync. Width	vs	1	2	254	Line
Vertical Sync. Back Porch	vbp	1	6	254	Line
Vertical Sync. Front Porch	vfp	1	8	--	Line

Note:

1. Typical value are related to the setting frame rate is 60Hz..

6.6 Reset timing

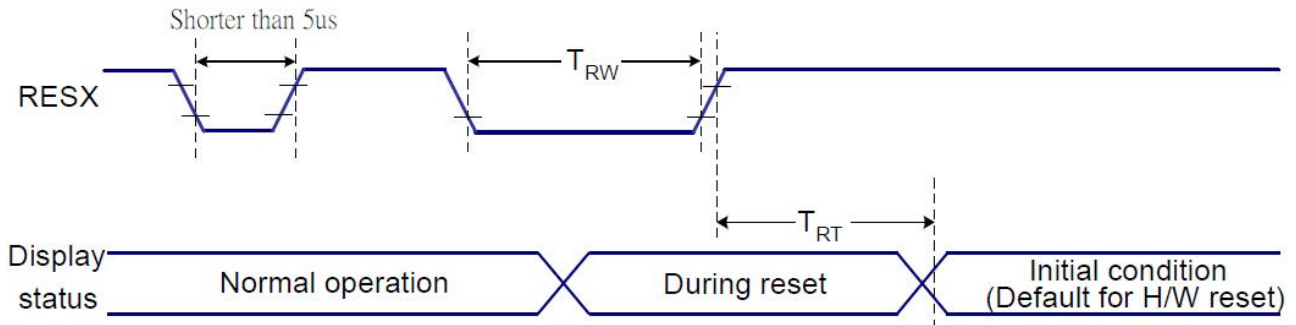


Figure6-5-1 Reset Timing

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a = -30$ to 70 °C

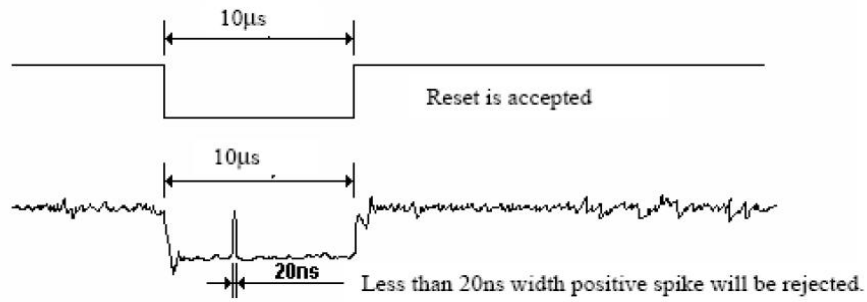
Signal	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	Reset pulse duration	10		us
	T_{RT}	Reset cancel		5 (Note 1, 5) 120 (Note 1, 6, 7)	ms ms

Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
- Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

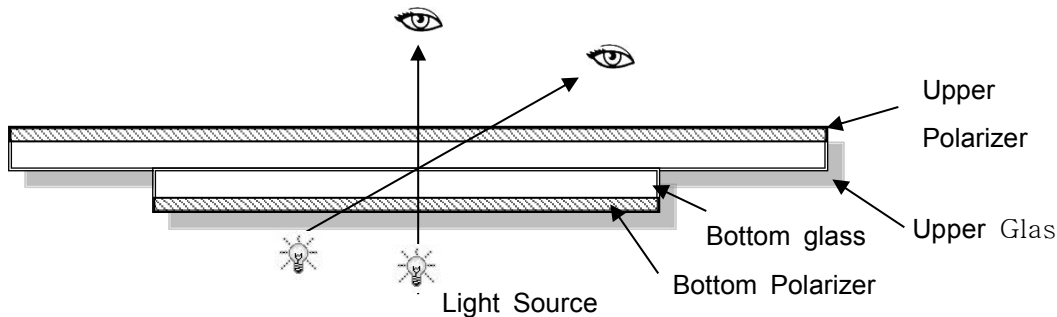
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

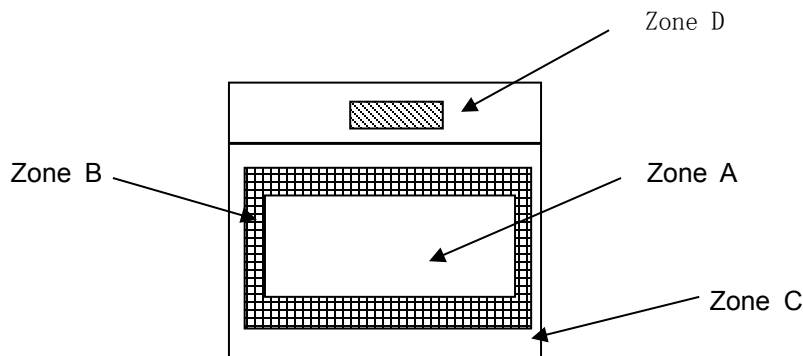
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

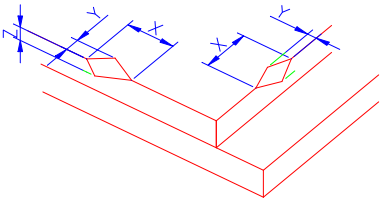
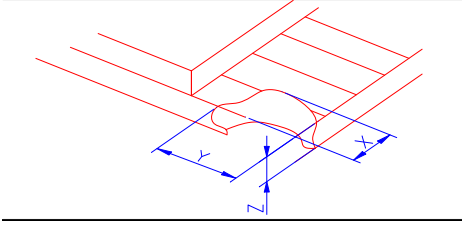
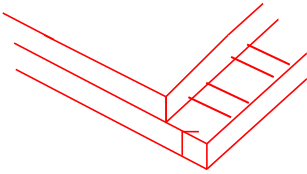
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

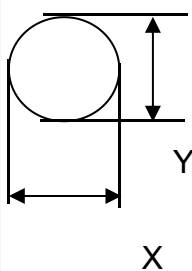
Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.




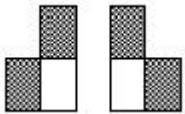
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.


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7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="756 667 1453 815"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
	(2)LCD corner broken	 <table border="1" data-bbox="836 1122 1374 1223"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>						

2.0	Spot defect	① light dot (black/white spot , pinhole, stain, etc.)			
		Acceptable Qty			
		Zone	A	B	C
		Size (mm)	Ignore		
$\Phi \leq 0.15$		Ignore			
	$0.15 < \Phi \leq 0.25$	3(distance ≥ 6 mm)			
	$0.25 < \Phi \leq 0.4$	2(distance ≥ 6 mm)			
	$\Phi > 0.4$	0			
	$\Phi = (X+Y)/2$	② Dim spot (light leakage, dent, dark spot, etc)			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.15$	Ignore			
	$0.15 < \Phi \leq 0.25$	3(distance ≥ 6 mm)			
	$0.25 < \Phi \leq 0.4$	2(distance ≥ 6 mm)			
	$\Phi > 0.4$	0			
		③ Polarizer accidented spot			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.2$	Ignore			
	$0.2 < \Phi \leq 0.5$	2(distance ≥ 6 mm)			
	$\Phi > 0.5$	0			
		④ Polarizer Bubble			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.2$	Ignore			
	$0.2 < \Phi \leq 0.4$	3(distance ≥ 6 mm)			
	$\Phi > 0.4$	0			

3.0	LCD Pixel defect	<p>Pixel bad points</p> <table border="1"> <thead> <tr> <th data-bbox="539 309 730 360">Item</th> <th data-bbox="730 309 1246 360">Zone A</th> <th data-bbox="1246 309 1497 360">Acceptable Qt</th> </tr> </thead> <tbody> <tr> <td data-bbox="539 360 730 521" rowspan="3">Bright dot</td> <td data-bbox="730 360 1246 416">Random</td> <td data-bbox="1246 360 1497 416">N≤2</td> </tr> <tr> <td data-bbox="730 416 1246 472">2 dots adjacent</td> <td data-bbox="1246 416 1497 472">N≤0</td> </tr> <tr> <td data-bbox="730 472 1246 521">3 dots adjacent</td> <td data-bbox="1246 472 1497 521">N≤0</td> </tr> <tr> <td data-bbox="539 521 730 689" rowspan="3">Dark dot</td> <td data-bbox="730 521 1246 577">Random</td> <td data-bbox="1246 521 1497 577">N≤2</td> </tr> <tr> <td data-bbox="730 577 1246 633">2 dots adjacent</td> <td data-bbox="1246 577 1497 633">N≤0</td> </tr> <tr> <td data-bbox="730 633 1246 689">3 dots adjacent</td> <td data-bbox="1246 633 1497 689">N≤0</td> </tr> <tr> <td data-bbox="539 689 730 1003">Distance</td> <td data-bbox="730 689 1246 1003"> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td> <td data-bbox="1246 689 1497 1003">5mm</td> </tr> <tr> <td colspan="2" data-bbox="539 1003 1246 1059">Total bright and dark dot</td> <td data-bbox="1246 1003 1497 1059">N≤4</td> </tr> </tbody> </table> <p>Note:</p> <p>A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.</p> <p>B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.</p> <p>C) 2 dot adjacent = 1 pair = 2 dots</p> <p>Picture:</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;">  <p>2 dot adjacent</p> </div> <div style="text-align: center;">  <p>2 dot adjacent</p> </div> <div style="text-align: center;">  <p>2 dot adjacent (vertical)</p> </div> <div style="text-align: center;">  <p>2 dot adjacent (slant)</p> </div> </div>	Item	Zone A	Acceptable Qt	Bright dot	Random	N≤2	2 dots adjacent	N≤0	3 dots adjacent	N≤0	Dark dot	Random	N≤2	2 dots adjacent	N≤0	3 dots adjacent	N≤0	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		N≤4
Item	Zone A	Acceptable Qt																							
Bright dot	Random	N≤2																							
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	3 dots adjacent	N≤0																							
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	2 dots adjacent	N≤0																							
	3 dots adjacent	N≤0																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		N≤4																							

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(m)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.03$</td> <td>Ignore</td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td>$0.03 < W \leq 0.04$</td> <td>$L \leq 3.0$</td> <td colspan="2">$N \leq 2$</td> </tr> <tr> <td>$0.04 < W \leq 0.05$</td> <td>$L \leq 2.0$</td> <td colspan="2">$N \leq 1$</td> </tr> <tr> <td>$W > 0.05$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length(m)	Acceptable Qty			A	B	C	$\Phi \leq 0.03$	Ignore	Ignore		Ignore	$0.03 < W \leq 0.04$	$L \leq 3.0$	$N \leq 2$		$0.04 < W \leq 0.05$	$L \leq 2.0$	$N \leq 1$		$W > 0.05$	Define as spot defect			
		Width(mm)			Length(m)	Acceptable Qty																						
			A	B		C																						
		$\Phi \leq 0.03$	Ignore	Ignore		Ignore																						
		$0.03 < W \leq 0.04$	$L \leq 3.0$	$N \leq 2$																								
$0.04 < W \leq 0.05$	$L \leq 2.0$	$N \leq 1$																										
$W > 0.05$	Define as spot defect																											
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite																										
6.0	Display color & Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.																										
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.																										

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	85°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-30°C, 96HR	
High Temperature Storage	85°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C,30 min ↔ 60°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80 _{cm} (MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

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9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10. Packing

---TBD-----

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